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10/059,176	01/31/2002	Hirokazu Hayashi	OKI.298	7695

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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/059,176	HAYASHI, HIROKAZU	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. JP 160692/2001.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/31/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 have been presented for examination based on the application filed on 31st January 2002.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. JP 160692/2001, filed on 29th May 2001.
3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in JP 246268/2001 on 14th August 2001. It is noted, however, that applicant has not filed a certified copy of the JP 246268/2001 application as required by 35 U.S.C. 119(b). Applicant has claimed priority to this application in the disclosure but has not provided a certified copy.
4. Foreign priority is acknowledged only for the Application No. JP 160692/2001, filed on 29th May 2001, until a certified copy of the Application No. JP 246268/2001 is filed.

Drawings

5. New corrected drawing(s) in compliance with 37 CFR 1.121(d) are required in this application because grammatical error in the Fig.14 (Element 50).
   Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

6. The incorporation of ***essential material*** in the specification by reference to an unpublished U.S. application, foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure to include the material incorporated by reference, if the material is relied upon to overcome any objection, rejection, or other requirement imposed by the Office. The amendment must be accompanied by a statement executed by the applicant, or a practitioner representing the applicant, stating that the material being inserted is the material previously incorporated by reference and that the amendment contains no new matter. 37 CFR 1.57(f).

   To overcome the above rejection a certified copy of the Application No. JP 246268/2001 should be filed.

7. Applicant is reminded of the proper language and format for an abstract of the disclosure.

> The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.
> The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Abstract starts with a language, which is not clear and concise. Examiner suggests using simple narrative phrase like "A method of modeling semiconductor process...".

8. **The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o).**

Correction of the following is required: The claim 1 discloses in the wherein section the phrase "mass of said impurity". This term lack antecedent basis as the specification never discloses absolute mass of the impurity rather discloses impurity in terms of density and change in density (Specification: Pg.12, Lines 19 –26).

Further, objection is made to the terminology used in the specification as the change in the impurity density and impurity density are disclosed as mass although they carry the dimensions [units/cubic centimeter].

Claims 1-7 are objected to for the reason disclosed above. Appropriate correction to the specification (throughout to correct the dimensions) and claims are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 1 recites the limitation "mass of said impurity ". There is insufficient antecedent basis for this limitation in the claim. Claim 3 also recites a similar phraseology. Claim 1 & 3 are rejected for the reasoning provided in the objection to the specification above. Claims 2, 4-7 are rejected based on the their dependency on claim 1.

10. Claims 6 & 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 6

Claim 6 discloses “a ninth step”. There are no previous eight steps disclosed in the claim or the preceding parent claim. Further claim 6 is rejected as lack of antecedent basis for the phrase “ninth step”. Further, claim 6 is rejected because it is not clear what “data of a magnitude of a reverse short channel effect” is being stored.

Regarding Claim 7

Claim 7 is vague because as best understood by the examiner SiO2 layer is understood as the insulating layer. Hence setting data for the SiO2 layer disposed opposite to the SiO2 is vague and is not clearly understood by the examiner. Further, examiner is not sure if the reference is being made to said SiO2 layer or some other insulating layer.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 1 & 5 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,594,625.

Application 10/059176 (HA '176 hereafter)	U.S. Patent No. 6,594,625 (HA '625 hereafter)
(Claim 1) A method for modeling a semiconductor device process, comprising: (a) setting data of an SiO.sub.2 layer;	(Claim1) A semiconductor modeling method comprising: a first step of storing data on an SiO.sub.2 layer;
(b) setting data of an Si layer brought in contact with said SiO.sub.2 layer;	a second step of storm data on an Si layer formed so as to be in contact with the SiO.sub.2 layer;
(c) setting a plurality of cells in said Si layer, and setting an amount of an impurity included in each of said cells;	a third step of dividing the Si layer into a plurality of regions, and setting an amount of impurity contained in the respective regions;
(d) setting an amount per unit time by which said impurity included in each of said cells moves to another cell;	a fourth step of setting an inter-regional migration amount of the impurity contained in the respective regions for a unit of time;
(e) setting data by which said cell in the vicinity of an interface of said SiO.sub.2 layer and said Si	a fifth step of constituting an impurity pileup part in a vicinity of an interface between the SiO.sub.2

layer is set as an impurity pileup portion;	and the Si layer;
(f) setting data of a position of a source or a drain in said Si layer; **(claim 5):** The method for modeling the semiconductor device process according to claim 1 wherein said step (f) comprises: assuming that a plurality of said sources or said drains exist in said Si layer; **and setting data in which the data of the position of specified said source or the data of the position of specified said drain is ignored.**	
g) calculating the amount of said impurity included in each of said cells for each unit time after processing the steps (a).about.(f), wherein a mass of said impurity moving to said pileup portion from each of said cells is determined as a function of a distance to said impurity pileup portion from each of said cells (hereinafter referred to as a distance r1), and a distance to said source or said drain from each of said cells (hereinafter referred to as a distance r2).	and a sixth layer of calculating impurity distribution in the respective regions for every unit of time after completion of the first, second, third, fourth and fifth steps, the semiconductor modeling method being carried out without using diffusion equations.

Although the conflicting method claims are not identical, they are not patentably distinct from each other because claim 5 negates the patentable distinction of the claim 1, i.e. the positions of drain and source are ignored, making the distance r2 a zero value. Thus, yielding a solution which is nearly identical to the claim 1 in HA '625.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to take claims of HA '625 patent and apply them to the instant application because such omission would have simplified the process of designing the model based system architecture.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,154,717 issued to Shingetaka Kumashiro (KU '717 hereafter), in view of Journal of Modeling and Simulation of Microsystems article "Physics-Based Threshold Voltage Modeling with Reverse Short Channel Effect" by K-Y Lim (LI 1999 hereafter).

Regarding Claim 1

KU '717 teaches (preamble & steps (a)(b)) a method of modeling semiconductor device process (KU '717: Col.1 Lines 7-14) by setting data for the SiO2 and Si layers brought in contact with each other (KU '717: Col.19 Lines47-48; Col.6 Lines 56-59). Further, KU '717 teaches (step (c)) setting plurality of cell in a layer (a mesh) with amount of impurity in each cell (KU '717: Col.19 Lines 52-57; Col.6 Lines 42-45). Further, KU '717 teaches (step (d) & (e)) setting diffusion rate on the impurities from one cell to another (KU '717: Col.19 Line 48) and setting up impurity pileup portion in a cell at the interface of SiO2 and Si (KU '717: Col.6 Lines 60-62).
Further, KU '717 teaches (step (g)) calculating the amount of impurity included in each cell after performing above-mentioned steps (KU '717: Col.6 Lines 63-64).

KU '717 does not teach step (f) explicitly.

LI 1999 teaches source and drain edges contributing to the reverse short channel effect and thus the affecting the impurities (LI 1999: Pg.52 Col.1 Lines 3-6). It would be obvious necessity to know the position of source and drain. Further, LI 1999 teaches that the rate of diffusion for the impurities is shown to be function of two distances (LI 1999: Pg.52, Equation 1).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **LI 1999** of **KU '717** to create a model of semiconductor device. The motivation to combine would have been that **KU '717** is simulating the impurity pileup in a semiconductor (KU '717: Abstract) and LI 1999 teaches to model the cause of the impurity diffusion by building joint vertical & lateral model for the phenomenon resulting from impurity pileup (LI 1999: Pg.51, Col.1 Lines 12-21; Pg.56 Conclusion).

Regarding Claim 2

LI 1999 teaches source or drain is set in the predetermined regions (LI 1999: Pg.51, Fig.1) and distance r2 is distance between cell and the predetermined region shown by the axes on the Fig.1.

Regarding Claim 3

KU '717 teaches meshing mechanism with mesh vertices (KU '717: Fig.6; Col6 Lines 60-62). Neither LI 1999 not KU '717 teach measuring distances in form of solid angle, hence impurity flux is also not shown in the form of solid angle.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made that the mesh is closed region representing a finite surface/volume and solid angle is just another way of measuring distances with one vertex as reference (cell) and other vertex (point at SiO2/Si interface or to the source/drain region)[1].

[1] "Solid Angle" definition from Mathworld.

Regarding Claim 4

KU '717 teaches emission (generation) and absorption (disappearance) rates with the time increments for each unit time (KU '717: Col.19 Lines 49-51, 58-61).

Regarding Claim 5

KU '717 teaches modeling a semiconductor without explicit knowledge of the position of the source or drain (KU '717: Col.1 Lines 7-14).

Regarding Claim 6

LI 1999 teaches storing data for magnitude the reverse channel effect and expressing the threshold voltage based on the impurity concentration (LI 1999: Pg.52 Equations 1, 2, 3, 3(a), 3(b), 3 (c)).

Regarding Claim 7

KU '717 teaches a method of modeling semiconductor device process (KU '717: Col.1 Lines 7-14) by setting data for the SiO2 and Si layers brought in contact with each other (KU '717: Col.19 Lines47-48; Col.6 Lines 56-59).

Conclusion

12. All claims are rejected.

13. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Thursday, July 21, 2005

JEAN R. HOMERE
PRIMARY EXAMINER